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EXAMINER	
FIEGLE, RYAN PAUL	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,759	BAXTER, MICHAEL A.	
	Examiner	Art Unit	
	Ryan P. Fiegle	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/29/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

2. Claims 23 and 42 are objected to because of the following informalities:

3. As per claim 23:

Claim 23 is dependent from claim 8. This is not congruent with the rest of the claim structure. While this is not against the rules, the examiner believes that the applicant meant for the claim to depend from claim 9 since depending from claim 8 would cause lack of antecedent basis for "processor." The examiner has assumed for the purposes of this office action that the claim is in fact dependent from claim 9. Appropriate correction is required.

4. As per claim 42:

"An" on line 2 should be "a." Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 9-23 and 35-44 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

7. As per claims 9 and 35:

The term "simple and balanced" is not defined within the specification.

8. As per claim 15:

The terms "sufficient" and "minimal enough" are not defined within the specification.

9. Any claims not referred to specifically are rejected to based on the deficiencies inherited by their parent claims.

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 9-23 and 35-44 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. As per claims 9 and 35:

The phrase "simple and balanced" renders the claim indefinite because it is a vague term that would not allow one of ordinary skill in the pertinent art to ascertain what was meant by the applicant.

13. As per claim 15:

The terms "sufficient" and "minimal enough" renders the claim indefinite because it is a vague term that would not allow one of ordinary skill in the pertinent art to ascertain what was meant by the applicant.

14. Any claims not referred to specifically are rejected to based on the deficiencies inherited by their parent claims.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 9, 10, 12-16, 21, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gadre et al. (US Patent 6,308,253) (hereafter referred to as Gadre).

17. As per claim 9:

Gadre teaches a system-on-chip, comprising:

a reduced instruction set computer processor implemented on a field programmable gate array fabric (Gadre: column 3, lines 2-5); and

a simple and balanced instruction set utilizing a minimal amount or resources from the field programmable gate array fabric (Gadre: column 8, lines 64-67; column 9, lines 1-16),

wherein the processor is synthesizable from hardware description language (Gadre: column 4, line 67; column 5, lines 1-2).

While Gadre does not specifically disclose an instruction set with 32 instructions, he does comment that a "small number of instructions" are used (Gadre: column 3, lines 2-5). It would have been obvious to one of ordinary skill in the art to make this 32 instructions since it is a power of 2 and is an optimal number for a small instruction set.

18. As per claim 10:

The system-on-chip of claim 9, wherein the same size is 32 bits (Gadre: Figures 7 and 8) (All instructions shown in the figures are 32 bits).

19. As per claim 12:

The system-on-chip of claim 9, wherein a series of bitfield layouts of machine words are arranged and constructed for compatibility with on-chip intellectual property cores (Gadre: column 4, lines 59-67; column 5, lines 1-10; column 6, lines 48-50).

20. As per claim 13:

The system-on-chip of claim 12, wherein the series of bitfield layouts are arranged and constructed for use with standard processor buses (Gadre: column 6, lines 52-57).

21. As per claim 14:

The system-on-chip of claim 9, wherein the processor includes at least 16 general purpose registers (Gadre: Figure 8) (There is 32 registers in Gadre) and 7 special purpose registers (Gadre Figure 5, items 178, 170, 164, and 176) (Item 176 can be duplicated n times and thus only one more would be needed to make 7 special purpose registers).

22. As per claim 15:

The system-on-chip of claim 9, wherein the processor includes a sufficient number of registers for C compiler functionality yet minimal enough for efficient field programmable gate array (FPGA) realization.

One of ordinary skill in the pertinent art would agree that 32 registers would provide sufficient storage for C register allocation while the latency of the register file would be low.

23. As per claim 16:

The system-on-chip of claim 9, wherein bitfield layouts for instruction formats and instruction ordering are arranged for efficient use of FPGA resources (Gadre: column 4, lines 59-67; column 5, lines 1-10).

24. As per claim 21:

The system-on-chip of claim 9, wherein the processor is based on a 32-bit architecture (Gadre: Figures 7 and 8).

25. As per claim 23:

The system-on-chip of claim 9, wherein the processor is based on one among a 16-bit, a 32-bit a 64-bit, a 128-bit, a 256-bit, a 512-bit and a 1024-bit architecture (Gadre: Figures 7 and 8).

26. As per claim 24:

Claim 24 recites the method of claim 9 with the same limitations and is rejected for the same reasons.

27. Claims 1-5, 7, 8, 11, 18- 20, 22, 25-33, 35-38 and 42-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gadre in view of Dao (US Patent 3,838,393)

and in view of Ito (US Patent 4,829,460) and in view of Gove et al. (US Patent 5,606,250) (hereafter referred to as Gove).

28. As per claim 1:

Gadre teaches a RISC architecture implemented on a programmable logic device (Gadre: column 3, lines 2-5).

Ito teaches a parallel bit shifter capable of reversible (Ito: column 6, lines 39-42) shifts and bit reversals (Ito: column 5, lines 7-9) while Gadre does not disclose a shifter.

Gadre teaches a DSP (Gadre: column 4, lines 50-53). Shifters are used in DSP functioning (Ito: column 1, lines 11-15). In addition Ito is implemented on an IC for easy integration into Gadre's programmable device (Ito: Abstract).

Therefore, it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention that applying Ito to Gadre would provide Gadre the benefit of performing shift functions in DSPing.

Dao teaches a Reed-Muller Boolean unit (Dao: column 3, lines 49-57) while Gadre does not.

Reed-Muller units are well known in the art to perform error correction. Dao in particular does parity checking as well as complex Boolean functions (Dao: column 1, lines 18-25). Gadre does DSPing with communications (Gadre: Figure 1). In addition Dao is implemented on an IC for easy integration into Gadre's programmable device (Dao: column 1, lines 57-59).

Therefore, it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention that applying Dao to Gadre would provide the benefit of error checking in communication functions.

Gove teaches a variety of immediate instructions that, via constant modes, variously manipulates distribution of a set of literal bits of a half-word literal field from an instruction word across a full-length data word (Gove: column 95, OR; column 103, Shift Left) while Gadre does not.

Gove states that, "it is desirable to design an entire parallel processor system, such as an image processor, on a single silicon chip while maintaining the system flexible enough to satisfy wide ranging and constantly changing operational criteria," (Gove: column 3, lines 6-9).

Gadre also states that it is desirable to implement parallel DSP chips onto the same integrated circuit device (Gadre: column 1, lines 53-57).

Therefore, it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention to apply Gove to Gadre to design an entire parallel processor system, such as an image processor, on a single silicon chip while maintaining the system flexible enough to satisfy wide ranging and constantly changing operational criteria.

29. As per claim 2:

The reduced instruction set computer architecture of claim 1, wherein the parallel bit shifter is a parallel 32-bit shifter (Ito: column 6, lines 28-32).

30. As per claim 3:

Ito teaches a parallel bit shifter ranked into three sections (Ito: Figure 3) while the applicant claims four. Because Ito teaches a parallel bit shifter that performs the operations of claim 1, it is apparent that the only difference between the two is that the applicant has separated one of the logic sections in Ito.

Since making parts separable has been found in In re Dulberg, 289 F.2d 522, 523, 129 USPQ 348, 349 (CCPA 1961), to not provide a patentable distinction, Ito teaches the limitations of claim 3.

31. As per claim 4:

The reduced instruction set computer architecture of claim 3, wherein the parallel bit shifter further comprises a split shift direction control signal applied on at least two of the four sections (Ito: column 3, lines 21-23).

32. As per claim 5:

One of ordinary skill in the pertinent art would have recognized that a Boolean function and its inverse only differ by a single transistor. If it was found to be advantageous to be able to find the inverse of the Boolean functions performed by Dao's Reed-Boolean unit, one of ordinary skill in the pertinent art would have found it obvious to add a latch controlled by a single bit which determines whether that single transistor is functional or not.

33. As per claim 7:

The reduced instruction set computer architecture of claim 1, wherein the immediate instruction function treats the half-word literal field as one among a lower-half, an upper-half (Gove: column 95, OR), a zero-filled word, a one-filled word, a sign-

extended word, or a replicated 1-bit for 2-bits word (Gove: column 53: lines 25-29) (zero-filled, one-filled, sign-extended and replicated 1-bit for 2-bits are all the same thing. If a number is positive it will be zero-filled sign-extended, if it is negative it will be 1-filled sign extended. The MSB is replicated to two bits for sign extension.)

34. As per claim 8:

The reduced instruction set architecture of claim 7, wherein the constant modes of the immediate instruction function include composite immediate instructions selected form the group of instructions comprising AND_FILL_LOW (Gove: column 69, AND) (AND is AND_FILL_LOW because a high half-word can be selected; the low half-word of the destination register will have to be filled), OR_LOW (Gove: column 95, OR) (OR is OR_LOW because it can select a low half-word), XOR_LOW (Gove: column 115, XOR) (XOR is XOR_LOW because it can select a low half-word), ADD_LOW (Gove: column 65, ADD) (ADD is ADD_LOW because it can select a low half-word), AND_FILL_HIGH (Gove: column 69, AND) (AND is AND_FILL_HIGH because a low half-word can be selected; the high half-word of the destination register will have to be filled), OR_HIGH (Gove: column 95, OR) (OR is OR_HIGH because it can select a high half-word), XOR_HIGH (Gove: column 115, XOR) (XOR is XOR_HIGH because it can select a high half-word), ADD_HIGH (Gove: column 65, ADD) (ADD is ADD_HIGH because it can select a high half-word), AND_DUPLEX (Gove: column 69, AND) (AND is AND_DUPLEX because it takes two operands), OR_DUPLEX (Gove: column 95, OR) (OR is OR_DUPLEX because it takes two operands), ADD_DUPLEX (Gove: column 65, ADD) (ADD is ADD_DUPLEX because it uses two source operands), AND_SIGN

(Gove: column 69, AND) (AND is AND_SIGN because it sets the Z bit, a signal or a sign, to indicate the result.), OR_SIGN (Gove: column 95, OR) (OR is OR_SIGN because it sets the Z bit, a signal or a sign, to indicate the result.), XOR_SIGN (Gove: column 115, XOR) (XOR is XOR_SIGN because it sets the Z bit, a signal or a sign, to indicate the result.), and ADD_SIGN (Gove: column 65, ADD) (ADD is ADD_SIGN because it can set a negative bit).

35. Gadre teaches claim 9 for the reasons stated above.

36. As per claim 11:

The system-on-chip of claim 9, wherein one instruction of the instruction set is a reserved for future use instruction (Gove: column 44, lines 26-27) (The fact that an illegal opcode can exist means that some opcodes have not been assigned and therefore can be used for future use. The motivation to combine Gadre with Gove is shown above.).

37. Gadre teaches claim 9 for the reasons stated above.

38. As per claim 18:

The system-on-chip of claim 9, wherein instruction formats include a balance of single and paired instructions well-suited for a C runtime software environment, such that instruction sequences required to implement C language constructs naturally break into instruction sequences comprising one or two instructions.

Gove teaches his immediate instruction function being 128 bits, or four words. However, Gadre is a RISC processor (Gadre: column 3, lines 2-5). One of ordinary skill in the pertinent art would have recognized that when Gove is applied to Gadre for the

reasons listed above, that the immediate instruction functions would have to be cracked into uOPs grouped together to complete the function. When the instructions are broken into uOPs, the instruction sequences required to implement C language constructs would naturally break into instruction sequences comprising one or two instructions.

39. As per claim 19:

It is inherent that cracking Gove's instructions into uOPs when applied to Gadre will reduce interrupt latency. This is because of the basic concept that reduced, simple uOPs reduce CPI. An instruction in the execution phase of a pipeline must complete before an interrupt can be serviced. If one or two simple uOPs are executed in one cycle, then an interrupt will be serviced faster than if a massive complex instruction that could spend many cycles in the execution phase is issued.

40. As per claim 20:

It is inherent that the reduced, simple instructions of Gadre will reduce the overhead since it will require less decoding. They will also facilitate interrupt driver software design directly in the C language since RISC compilers are easier to write than CISC.

41. Gadre teaches claim 9 for the reasons stated above.

42. As per claim 22:

The system-on-chip of claim 9, wherein the processor comprises at least one among a balanced instruction set; a set of six instruction forms; a byte-addressed 32-bit address space; addressing by word, half-word, or byte; a little endian byte ordering (Gove: column 55, lines 8-10).

43. Gadre teaches claim 24 for the reasons stated above.

44. As per claim 25:

Claim 25 recites the method of claim 11 with the same limitations and is rejected for the same reasons.

45. Gadre teaches claim 24 for the reasons stated above.

46. As per claim 26:

The method of claim 24, wherein one instruction of the instruction set is an immediate instruction that, via constant modes, variously manipulates distribution of a set of literal bits of a half-word literal field from an instruction word across a full-length data word (Gove: column 95, OR) (The motivation to apply Gove to Gadre is shown above).

47. Gadre teaches claim 24 for the reasons stated above.

48. As per claim 27:

The method of claim 24, wherein embedding the processor core comprises configuring the field programmable gate array to include a parallel bit shifter capable of reversible shifts and bit reversals (Ito: column 5, lines 7-9; column 6, lines 39-42) and a Reed-Muller Boolean unit coupled to the parallel bit shifter (Dao: column 3, lines 49-57) (The motivation for applying Ito and Dao to Gadre is provided above.).

49. As per claim 28:

Gadre teaches a RISC architecture implemented on a programmable logic device (Gadre: column 3, lines 2-5), comprising:

a parallel bit shifter capable of reversible (Ito: column 6, lines 39-42) shifts and bit reversals (Ito: column 5, lines 7-9) (Motivation to combine Ito to Gadre is provided above);

a Reed-Muller Boolean unit (Dao: column 3, lines 49-57) (Motivation to combine Dao to Gadre is provided above) coupled to the parallel bit shifter; and

an immediate instruction function used in conjunction with the parallel bit shifter and Reed-Muller Boolean unit, the immediate instruction function having N possible modes and having a plurality of instruction bits, with half of the plurality of instruction bits of the instruction allocated to immediate data (Gove: column 95, OR; column 103, Shift Left) (Motivation for combining Gove to Gadre is provided above).

Gove does not teach his immediate instruction function being a single word. However, as noted above, Gadre is a RISC processor (Gadre: column 3, lines 2-5). One of ordinary skill in the pertinent art would have recognized that when Gove is applied to Gadre for the reasons listed above, that the immediate instruction functions would have to be cracked into uOPs grouped together to complete the function. When the instructions are broken into uOPs, the immediate instruction function would be a single word and the immediate would take up half the word.

50. As per claim 29:

Claim 29 recite the same limitations as claim 8 and is rejected for the same reasons.

51. As per claim 30:

The reduced instruction set computer architecture of claim 28, wherein the immediate instruction function further includes a predetermined number of separate operation sub-modes (See the sub-modes referred to in claim 8.).

52. As per claim 31:

The reduced instruction set architecture of claim 30, wherein the separate operation sub-modes are selected from the group of arithmetic logical operating modes comprising AND, OR, XOR, and ADD, and

wherein the AND mode is used for at least one zeroing unwanted literal bits and masking of an operand (Gove: column 31, lines 4-7) (Though Gove does not explicitly teach using an AND gate for masking, such is inherent based on the truth table of an AND gate. To be able to mask part of an operand and keep the total number of bits, one of ordinary skill in the pertinent art would agree that the most efficient and simplest way to do so is to AND the operand with a mask.), the OR mode is used for inserting desired literal bits into a selected general purpose register (Gove: column 56, lines 37-40), the XOR mode used for complementing select bits of an operand in a general purpose register when necessary (Gove: column 31, lines 11-15), and the ADD mode is used for immediate arithmetic operation (Gove: column 56, lines 37-40).

53. As per claim 32:

The reduced instruction set computer architecture of claim 28, wherein the immediate instruction function further includes a predetermined number of separate bit mask sub-modes.

As addressed in the rejection in reference to claim 8, Gadre in combination with Gove teach AND, OR, XOR and ADD with six varying sub-modes.

54. As per claim 33:

The reduced instruction set computer architecture of claim 32, wherein the separate bit mask sub-modes are selected from the group of bit mask sub-modes comprising FILL LOW, FILL HIGH, LOW, HIGH, DUPLEX, and SIGN bit masks.

As referenced in the rejection of claim 8, Gadre combined with Gove teach these six sub-modes.

55. As per claim 35:

Gadre teaches a system-on-chip, comprising:

a reduced instruction set computer processor implemented on a programmable logic device fabric (Gadre: column 3, lines 2-5);

a simple and balanced instruction set utilizing a minimal amount of resources from the field programmable gate array fabric (Gadre: column 8, lines 64-67; column 9, lines 1-16) , wherein the processor is synthesizable from hardware description language (Gadre: column 4, line 67; column 5, lines 1-2).

Gadre does not teach a horizontally scalable immediate instruction using multiple vectorized versions of an N-bit architecture (Gove: column 95, OR; column 103, Shift Left).

The reasons for combining Gadre and Gove are provided above.

56. As per claim 36:

The system-on-chip of claim 35, wherein the horizontally scalable immediate instruction concurrently uses multiple vectorized versions of the N-bit architecture (Gove: column 95, OR; column 103, Shift Left).

57. As per claim 37:

The system-on-chip of claim 35, wherein the N-bit architecture can be selected among multiple 16-bit, 32-bit, 64-bit, 128-bit, 256-bit, 512-bit and 1024-bit vectorized versions (Gove: column 95, OR; column 103, Shift Left) (Gove's immediate instruction uses 128 bits).

58. As per claim 38:

The system-on-chip of claim 35, wherein the N-bit architecture can be selected among multiple 18-bit, 36-bit, 72-bit, 144-bit, 288-bit, 576-bit and 1152-bit vectorized versions (Gove: column 95, OR; column 103, Shift Left) (Although Gove's immediate instruction uses 128 bits, it has been found in In re Rose, 220 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955) that changing size does not make a patentable distinction.).

59. As per claim 42:

The system-on-chip of claim 35, wherein the instruction set further comprises a reserved for future use (rfu) instruction that enables vertically scalable architectural variants implemented on the field programmable gate array fabric (Gove: column 44, lines 26-27) (The fact that an illegal opcode can exist means that some opcodes have not been assigned and therefore can be used for future use.).

60. As per claim 43:

Gadre does not teach floating point instructions. However, it would be obvious to implement the rfu instructions of Gove to implement floating point instructions since their use and advantages are very well known in the art (Official Notice).

61. As per claim 44:

It would have been obvious to implement the rfu as an architecture extension in firmware since such is very well known in the art (IBM microcode was implemented as early as 1973) (Official Notice).

62. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gadre, Dao, Ito and Gove as applied to claim 1 above, and in view of Wakerly.

63. Gadre, Dao, Ito and Gove teach claim 1 for the reasons above.

64. As per claim 6:

Dao's Reed-Muller Boolean unit can accept four inputs. However, the purpose of Dao's invention is versatility in his unit to provide multiple functions (Dao: column 3, lines 45-57). Therefore, if it was found advantageous to select two of the four operands, it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention to use a multiplexer since multiplexers are cheap, easy to fabricate and well known by designers (Wakerly: 20).

65. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gadre as applied to claim 9 above, and in view of Parthasarathy et al. (US Patent 6,934,828).

66. Gadre teaches claim 9 for the reasons above.

67. As per claim 17:

Gadre does not teach the system-on-chip of claim 9, wherein instruction formats include a balance of single and paired instructions well-suited for compilation, such that after a first-issued instruction is considered by a compiler for issue, the compiler beneficially considers no more than 30 alternative instructions for a second-issued instruction to pair with the first-issued instruction.

All that is being described here is a 2-way dispatch out-of-order superscalar processor, which is very well known in the art as well as its advantages. One of ordinary skill in the pertinent art would have recognized that to support out-of-order processing a processor must possess an instruction window, a reorder buffer or a scoreboard to hold a predetermined number of decoded instructions. This number can vary; however, Parthasarathy et al. disclose that a 20-30-entry instruction window increases performance in a superscalar machine (Parthasarathy: column 1, lines 28-31).

Therefore it would have been obvious to one of ordinary skill in the pertinent art to make Gadre a 2-way dispatch out-of-order superscalar processor with an instruction window of 30 entries to increase performance.

Allowable Subject Matter

68. Claims 34 and 39-41 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

69. As per claim 34:

Gadre in combination with Gove, Ito and Dao cannot teach a LOW bit mask and a HIGH bit mask wherein the masks are used in filling a half word in a **pair** of words. They also cannot teach a duplex mode wherein the SIGN mode is used for creating nibbles, bytes and half-word masks.

70. As per claim 39:

Gadre in combination with Gove, Ito and Dao cannot teach generating two N-bit words of constant data using n N/2 bit immediate instruction having N/4 bits dedicated for immediate data. While Gove teaches an immediate instruction, and when combined with Gadre that instruction can be a single word wherein half the bits are immediate data, no reasonable combination can say that the data generated by these instructions are two separate N-bit words, where N would be 64 bits in the case of Gadre.

71. As per claim 40:

While Gove can teach FFT, no reasonable combination can teach the limitations of claim 39.

72. As per claim 41:

Claim 41 contains allowable subject matter because no reasonable combination can teach the limitations of claim 39.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan P. Fiegle whose telephone number is 571-272-5534. The examiner can normally be reached on M-F 12-8.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan P Fiegle
Examiner
Art Unit 2183

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100